

CD4541BC Programmable Timer

General Description

The CD4541BC Programmable Timer is designed with a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, output control logic, and a special power-on reset circuit. The special features of the power-on reset circuit are first, no additional static power consumption and second, the part functions across the full voltage range (3V–15V) whether power-on reset is enabled or disabled.

Timing and the counter are initialized by turning on power, if the power-on reset is enabled. When the power is already on, an external reset pulse will also initialize the timing and counter. After either reset is accomplished, the oscillator frequency is determined by the external RC network. The 16-stage counter divides the oscillator frequency by any of 4 digitally controlled division ratios.

Features

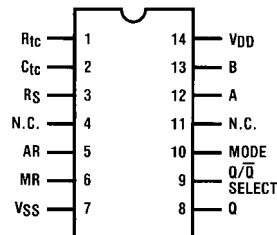
- Available division ratios 2^8 , 2^{10} , 2^{13} , or 2^{16}
- Increments on positive edge clock transitions
- Built-in low power RC oscillator ($\pm 2\%$ accuracy over temperature range and $\pm 10\%$ supply and $\pm 3\%$ over processing @ < 10 kHz)
- Oscillator frequency range = DC to 100 kHz
- Oscillator may be bypassed if external clock is available (apply external clock to pin 3)
- Automatic reset initializes all counters when power turns on
- External master reset totally independent of automatic reset operation
- Operates at 2^n frequency divider or single transition timer
- Q/\bar{Q} select provides output logic level flexibility
- Reset (auto or master) disables oscillator during resetting to provide no active power dissipation
- Clock conditioning circuit permits operation with very slow clock rise and fall times
- Wide supply voltage range—3.0V to 15V
- High noise immunity— $0.45 V_{DD}$ (typ.)
- 5V–10V–15V parameter ratings
- Symmetrical output characteristics
- Maximum input leakage $1 \mu A$ at 15V over full temperature range
- High output drive (pin 8) min. one TTL load

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| CD4541BCM | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4541BCN | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



N.C.—Not connected

Top View

Truth Table

| Pin | State | |
|-----|----------------------------------|-----------------------------------|
| | 0 | 1 |
| 5 | Auto Reset Operating | Auto Reset Disabled |
| 6 | Timer Operational | Master Reset On |
| 9 | Output Initially Low after Reset | Output Initially High after Reset |
| 10 | Single Cycle Mode | Recycle Mode |

Division Ratio Table

| A | B | Number of Counter Stages | Count |
|---|---|--------------------------|----------------|
| | | n | 2 ⁿ |
| 0 | 0 | 13 | 8192 |
| 0 | 1 | 10 | 1024 |
| 1 | 0 | 8 | 256 |
| 1 | 1 | 16 | 65536 |

Operating Characteristics

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state.

The RC oscillator frequency is determined by the external RC network, i.e.:

$$f = \frac{1}{2.3 R_{TC} C_{TC}} \text{ if } (1 \text{ kHz} \leq f \leq 100 \text{ kHz})$$

and $R_S \approx 2 R_{TC}$ where $R_S \geq 10 \text{ k}\Omega$

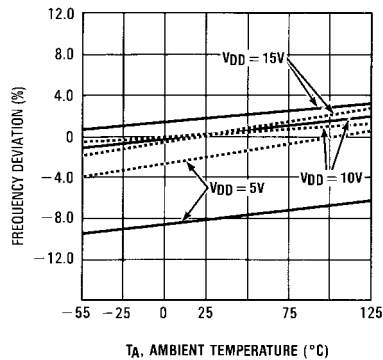
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2⁸, 2¹⁰, 2¹³, and 2¹⁶). The 2ⁿ counts as shown in the Division Ratio Table represent the Q output of the Nth stage of the counter. When A is "1", 2¹⁶ is selected for both states of B.

However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2⁸).

The Q/Q̄ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/Q̄ select pin is set to a "0" the Q output is a "0". Correspondingly, when Q/Q̄ select pin is set to a "1" the Q output is a "1".

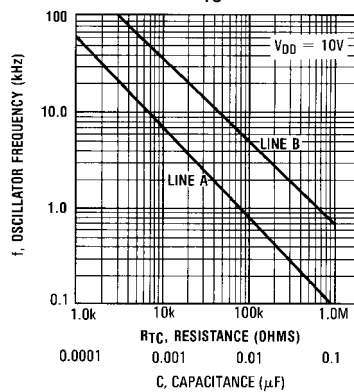
When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop resets (see Logic Diagram), counting commences and after 2ⁿ⁻¹ counts the RS flip-flop sets which causes the output to change state. Hence, after another 2ⁿ⁻¹ counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

Typical RC Oscillator Characteristics



Solid Line = $R_{TC} = 56 \text{ k}\Omega$, $R_S = 1 \text{ k}\Omega$ and $C = 1000 \text{ pF}$
 $f = 10.2 \text{ kHz}$ @ $V_{DD} = 10\text{V}$ and $T_A = 25^\circ$
 Dashed Line = $R_{TC} = 56 \text{ k}\Omega$, $R_S = 120 \text{ k}\Omega$ and $C = 1000 \text{ pF}$
 $f = 7.75 \text{ kHz}$ @ $V_{DD} = 10\text{V}$ and $T_A = 25^\circ$

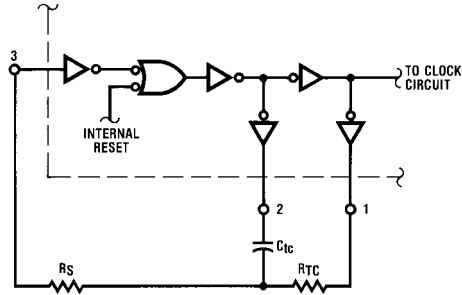
RC Oscillator Frequency as a Function of R_{TC} and C



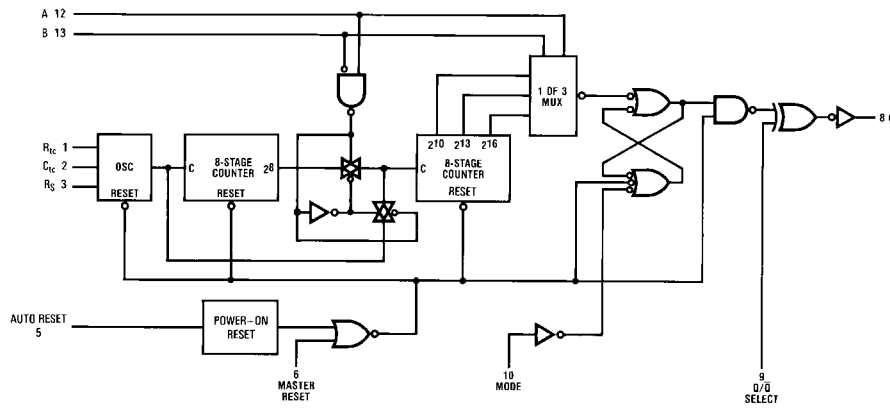
Line A: f as a function of C and ($R_{TC} = 56 \text{ k}\Omega$; $R_S = 120\text{k}$)
 Line B: f as a function of R_{TC} and ($C = 100 \text{ pF}$; $R_S = 2 R_{TC}$)

Operating Characteristics (Continued)

Oscillator Circuit Using RC Configuration



Logic Diagram



V_{DD} = Pin 14

V_{SS} = Pin 7

Absolute Maximum Ratings (Note 1)

(Note 2)

| | |
|-------------------------------------|--------------------------|
| Supply Voltage (V_{DD}) | -0.5V to +18V |
| Input Voltage (V_{IN}) | -0.5V to $V_{DD} + 0.5V$ |
| Storage Temperature Range (T_S) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature (T_L) | |
| (soldering, 10 seconds) | 260°C |

Recommended Operating Conditions (Note 2)

| | |
|-----------------------------|-----------------|
| Supply Voltage (V_{DD}) | 3V to 15V |
| Input Voltage (V_{IN}) | 0 to V_{DD} |
| Operating Temperature Range | -55°C to +125°C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 2)

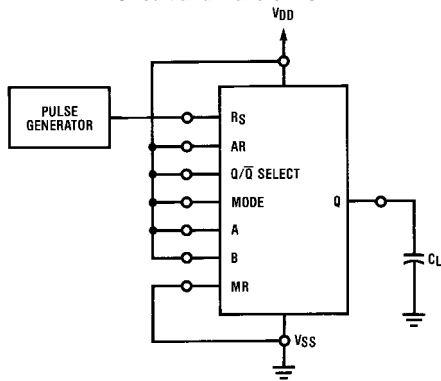
| Symbol | Parameter | Conditions | -55°C | | +25°C | | | +125°C | | Units |
|----------|---------------------------------------|---|-------|------|-------|------------|------|--------|---------|-------|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| I_{DD} | Quiescent Device Current | $V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS} | | 5 | | 0.005 | 5 | 150 | μA | |
| | | $V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS} | | 10 | | 0.010 | 10 | 300 | | |
| | | $V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS} | | 20 | | 0.015 | 20 | 600 | | |
| V_{OL} | LOW Level Output Voltage | $V_{DD} = 5V$ | | 0.05 | | 0 | 0.05 | 0.05 | V | |
| | | $V_{DD} = 10V$ | | 0.05 | | 0 | 0.05 | 0.05 | | |
| | | $V_{DD} = 15V$ | | 0.05 | | 0 | 0.05 | 0.05 | | |
| V_{OH} | HIGH Level Output Voltage | $V_{DD} = 5V$ | 4.95 | | 4.95 | 5 | | 4.95 | V | |
| | | $V_{DD} = 10V$ | 9.95 | | 9.95 | 10 | | 9.95 | | |
| | | $V_{DD} = 15V$ | 14.95 | | 14.95 | 15 | | 14.95 | | |
| V_{IL} | LOW Level Input Voltage | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | | 1.5 | | 2 | 1.5 | 1.5 | V | |
| | | $V_{DD} = 10V, V_O = 1.0V$ or $9.0V$ | | 3.0 | | 4 | 3.0 | 3.0 | | |
| | | $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$ | | 4.0 | | 6 | 4.0 | 4.0 | | |
| V_{IH} | HIGH Level Input Voltage | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | 3.5 | | 3.5 | 3 | | 3.5 | V | |
| | | $V_{DD} = 10V, V_O = 1.0V$ or $9.0V$ | 7.0 | | 7.0 | 6 | | 7.0 | | |
| | | $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$ | 11.0 | | 11.0 | 9 | | 11.0 | | |
| I_{OL} | LOW Level Output Current (Note 3) | $V_{DD} = 5V, V_O = 0.4V$ | 2.85 | | 2.27 | 3.6 | | 1.6 | mA | |
| | | $V_{DD} = 10V, V_O = 0.5V$ | 4.16 | | 4.0 | 9.0 | | 2.8 | | |
| | | $V_{DD} = 15V, V_O = 1.5V$ | 19.3 | | 15.6 | 34.0 | | 10.9 | | |
| I_{OH} | HIGH Level Output Current (Note 3) | $V_{DD} = 5V, V_O = 2.5V$ | 7.96 | | 6.42 | 130 | | 4.49 | mA | |
| | | $V_{DD} = 10V, V_O = 9.5V$ | 4.19 | | 3.38 | 8.0 | | 2.37 | | |
| | | $V_{DD} = 15V, V_O = 13.5V$ | 16.3 | | 13.2 | 30.0 | | 9.24 | | |
| I_{IN} | Input Current | $V_{DD} = 15V, V_{IN} = 0V$ | | -0.1 | | -10^{-5} | -0.1 | -1.0 | μA | |
| | | $V_{DD} = 15V, V_{IN} = 15V$ | | 0.1 | | 10^{-5} | 0.1 | 1.0 | | |

Note 3: I_{OH} and I_{OL} are tested one output at a time.

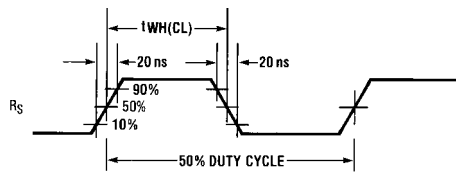
| AC Electrical Characteristics (Note 4) | | | | | | |
|---|---|--|-------------------|-------------------|-------------------|-------|
| T _A = 25°C, C _L = 50 pF (refer to test circuits) | | | | | | |
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| t _{TLH} | Output Rise Time | V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V | | 50 30 25 | 200 100 80 | ns |
| t _{THL} | Output Fall Time | V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V | | 50 30 25 | 200 100 80 | ns |
| t _{PLH} , t _{PHL} | Turn-Off, Turn-On Propagation Delay, Clock to Q (2 ⁸ Output) | V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V | | 1.8 0.6 0.4 | 4.0 1.5 1.0 | μs |
| t _{PHL} , t _{PLH} | Turn-On, Turn-Off Propagation Delay, Clock to Q (2 ¹⁶ Output) | V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V | | 3.2 1.5 1.0 | 8.0 3.0 2.0 | μs |
| t _{WH(CL)} | Clock Pulse Width | V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V | 400 200 150 | 200 100 70 | | ns |
| f _{CL} | Clock Pulse Frequency | V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V | | 2.5 6.0 8.5 | 1.0 3.0 4.0 | MHz |
| t _{WH(R)} | MR Pulse Width | V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V | 400 200 150 | 170 75 50 | | ns |
| C _I | Average Input Capacitance | Any Input | | 5.0 | 7.5 | pF |
| C _{PD} | Power Dissipation Capacitance (Note 5) | | | 100 | | pF |
| <p>Note 4: AC Parameters are guaranteed by DC correlated testing.</p> <p>Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics application note: AN-90.</p> | | | | | | |

Test Circuits and Waveforms

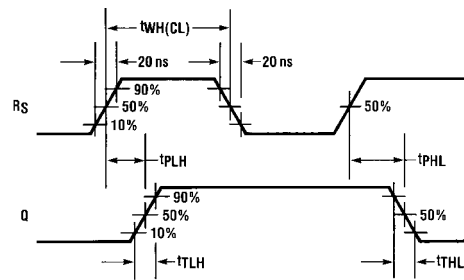
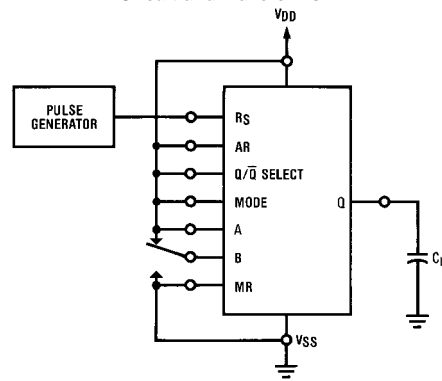
Power Dissipation Test Circuit and Waveforms



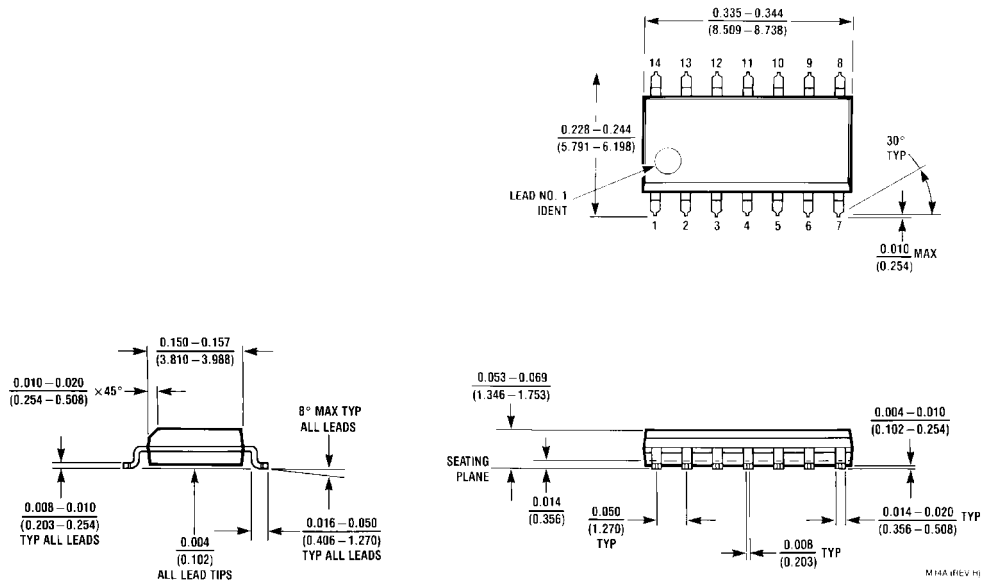
(R_{TC} and C_{TC} outputs are left open)



Switching Time Test Circuit and Waveforms



Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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